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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/803,311	03/18/2004	Shawn D. Rogers	10599/131	5776

7590 07/27/2007

Brinks Hofer Gilson & Lione
P.O. Box 10395
Chicago, IL 60610

EXAMINER	
NGUYEN, HOA CAO	
ART UNIT	PAPER NUMBER
2841	

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07/27/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/803,311	ROGERS ET AL.	
	Examiner	Art Unit	
	Hoa C. Nguyen	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1-68* is/are pending in the application.

4a) Of the above claim(s) *2,4-7 and 11-68* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3, and 8-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 2, 4-7, and 11-68 withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention group, there being no allowable generic or linking. Applicants' selection of Species 3, figure 3, on which claims 1, 3, and 8-10 are readable with traverse, in the reply filed on 3/1/07 is acknowledged. The traversal is on the ground that the Examiner has not made out any case that the additional dependent claims 60-68 have increased the complexity of the application. The argument is not persuasive, because each Species contains additional limitation(s) comparing to the others. Therefore, the search for every limitation for each Species is the burden for the Examiner.

Thus, the requirement is still deemed proper and is therefore made **FINAL**.

Claims 1, 3, and 8-10 are treated on the merits in this Office Action.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 3, and 8-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Davidson (US 6400576).

Regarding claim 1, as shown in figures 2-4, Davidson discloses a multilayer board 40 (LGA package, col.5:46) comprising:

(a) a surface area 50 (upper surface, col.1:32) where an electrical device 20 (IC, col.1:35) is mountable; and

(b) an array of capacitive elements 190 (col.7:34-54) at least partially surrounding the electrical device (beneath the IC 40).

Regarding claim 3, Davidson discloses the capacitive elements 190 comprise at least one of capacitors (col.7:34-54) or conductive patches (inherently formed in within each capacitor).

Examiner remarks: Applicants should be noted that all capacitive elements including discrete capacitors (chip capacitor for example) are formed by at least two conductive layers namely patches, pads, or electrodes sandwiched at least a layer of dielectric material in between.

Regarding claim 8, Davidson discloses a characteristic (capacitance) of the capacitive elements in the array changes with a distance from the electrical device (see different capacitance, different self-resonant frequency, col.7:34-54).

Regarding claims 9 and 10, as Davidson discloses the capacitive elements having different capacitance, therefore it is inherently that the conductive plates of the capacitors (conductive layers - patches, pads, or electrodes, see claim 3 above) are also changed in size and effectively to the shape of the plates (patches).

4. Claims 1, 3, and 8-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakamura (US 20020023342).

Regarding claim 1, as shown in figure 1, Nakamura discloses a multilayer board 1 (multi-chip module, par.56) comprising:

(a) a surface area 2X (main surface, par.56) where an electrical device 10 (semiconductor chip, par.56) is mountable; and

(b) an array of capacitive elements 17/18 (plurality of chip capacitors, par.56) at least partially surrounding the electrical device (left and right side of the chip 10).

Regarding claim 3, as clearly shown in figure 1, Nakamura discloses the capacitive elements 17/18 comprise at least one of capacitors (or conductive patches inherently formed in within each capacitor).

Examiner remarks: Applicants should be noted that all capacitive elements including discrete capacitors (chip capacitor for example) are formed by at least two conductive layers namely patches, pads, or electrodes sandwiched at least a layer of dielectric material in between.

Regarding claim 8, Nakamura discloses a characteristic (capacitance, size of capacitor) of the capacitive elements in the array changes (at least with size of the capacitor) with a distance from the electrical device (capacitor 17 is different from capacitor 18, as shown in the figure, and both are in different distance from the electrical device).

Regarding claims 9 and 10, as Nakamura discloses at least two capacitor sizes, capacitor 18 is larger than capacitor 17), therefore it is inherently that the conductive plates of the capacitor (conductive layers - patches, pads, or electrodes, see

claim 3 above) are also changed in size and effectively to the shape of the plates (patches).

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoa C. Nguyen whose telephone number is 571-272-8293. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on 571-272-1984. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Hoa C. Nguyen
7/18/07

DEAN A. REICHARD 7/20/07
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800